CLAIMS

I claim:

1. An apparatus for the construction of one of a microscale and nanoscale device, comprising:

a first region comprising a diaphragm, the diaphragm comprising a first insulator material, the diaphragm having a top surface and a bottom surface,

a substrate region comprising semiconductor material supporting the first region, the semiconductor material comprising a rigid frame laterally surrounding the diaphragm,

a substrate cavity region beneath the diaphragm,

a third region comprising a third insulator material, the third region being disposed atop the diaphragm, the third region being substantially thicker than the diaphragm and having a third cavity therethrough exposing a portion of the top surface of the diaphragm, the exposed portion of the top surface of the diaphragm being suitable for fabrication of one of a microscale and a nanoscale device.

2. A structure as recited in claim 1, wherein the one of a microscale and a nanoscale device comprises a first hole extending through the diaphragm.

3. A structure as recited in claim 1, wherein the one of a microscale and a nanoscale device comprises a nanopore.

4. A structure as recited in claim 1, further comprising a second region comprising a second insulator material laterally surrounding the first region, and having an upper surface substantially flush with the bottom surface of the first region, the second region being substantially thicker than the first region.

5. A structure as recited in claim 1, further comprising a fourth region comprising a fourth insulator material disposed atop the third region, the fourth region being substantially thicker than the first region and having a fourth cavity therethrough

exposing a portion of the top surface of the third region surrounding the third cavity.

6. A structure as recited in claim 1, further comprising a fifth material, the fifth material comprising a bottom layer portion of the diaphragm.
7. A structure as recited in claim 1, further comprising a sixth region comprising a sixth insulator material disposed atop the substrate region.
8. A structure as recited in claim 1, wherein the first region comprises one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a polymer, a semiconductor, and a metal.
9. A structure as recited in claim 1, wherein the first region comprises silicon nitride.
10. A structure as recited in claim 1, wherein the third region comprises one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a semiconductor, and a metal.
11. A structure as recited in claim 4, wherein the fourth region comprises one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a semiconductor, and a metal.
12. A structure as recited in claim 5, wherein the fourth region comprises one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a semiconductor, and a metal.
13. A structure as recited in claim 1, wherein the diaphragm is from 50 nm to 500 nm in thickness.
14. A structure as recited in claim 1, wherein the diaphragm is about 200 nm thick.
15. A structure as recited in claim 1, wherein the third region is from 1 to 50 micrometers in thickness.
16. A structure as recited in claim 1, wherein the third region is about 2 micrometers thick.

17. A structure as recited in claim 4, wherein the second region is from 1 to 20 micrometers in thickness.

18. A structure as recited in claim 4, wherein the second region is from about 10 micrometers thick.

19. A structure as recited in claim 5, wherein the fourth region is from 1 to 50 micrometers in thickness.

20. A structure as recited in claim 5, wherein the fourth region is about 25 micrometers thick.

21. A structure as recited in claim 1, wherein the semiconductor material comprises one of silicon, germanium, and gallium arsenide.

22. A structure as recited in claim 6 wherein the fifth material comprises one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a semiconductor, and a metal.

23. A structure as recited in claim 7 wherein the sixth material comprises one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a semiconductor, and a metal.

24. A structure as recited in claim 1, further comprising one of electrical leads and microfluidic leads, said lead being disposed at a location comprising one of beneath the third region, atop the third region, atop the fourth region, beneath the plane of the bottom surface of the diaphragm, and within the substrate cavity.

25. A structure as recited in claim 24, further comprising an electrical lead comprising one of a metal, a silicide, an organic conductor, a superconductor, aluminum, gold, platinum, palladium, iridium, copper, chromium, and nickel.

26. A structure as recited in claim 24, further comprising a microfluidic lead comprising one of a polymer, photoresist, SU8 photoresist, epoxy, polyimide, Parylene®, a silicone polymer, silicon dioxide, silicon nitride, silicon oxynitride, silicon-rich silicon nitride, TEOS oxide, plasma nitride, an insulator, a semiconductor, and a metal.

27. A method of fabricating an apparatus for the construction of one of a microscale and nanoscale device, comprising:

providing a semiconductor substrate having upper and lower major surfaces,

providing a first region comprising a first insulator material atop the semiconductor substrate,

forming a substrate cavity region beneath the first region, thereby forming a diaphragm comprising the first material,

forming a third region comprising a third insulator material atop the first region, the third region being substantially thicker than the first region, and

forming a third cavity through the third region, thereby exposing portion of the top surface of the diaphragm, the exposed portion of the top surface of the diaphragm being suitable for fabrication of one of a microscale and a nanoscale device..

28. A method as recited in claim 28, wherein the one of a microscale and a nanoscale device comprises a first hole extending through the diaphragm.

29. A method as recited in claim 28, wherein the one of a microscale and a nanoscale device comprises a first hole a nanopore.

30. A method as recited in claim 28, further comprising providing a second region comprising a second insulator material laterally surrounding the first region, and having an upper surface substantially flush with the bottom surface of the first region, the second region being substantially thicker than the first region.

31. A method as recited in claim 28, further comprising providing a fourth region comprising a fourth insulator material disposed atop the third region, the fourth region being substantially thicker than the first region, and forming a fourth cavity through the fourth region thereby exposing a portion of the top surface of the third region surrounding the third cavity.

32. A method as recited in claim 28, further comprising providing a fifth material, the fifth material comprising a bottom layer portion of the diaphragm.

33. A method as recited in claim 28, further comprising providing a sixth region comprising a sixth insulator material disposed atop the substrate region.

34. A method as recited in claim 28, further comprising providing one of electrical leads and microfluidic leads, said lead being disposed at a location comprising one of beneath the third region, atop the third region, atop the fourth region, beneath the plane of the bottom surface of the diaphragm, and within the substrate cavity.